

EER-018
Fall, 1997
Review Problems - Combinational Logic

Name _____

1. Perform the binary addition, subtraction, and multiplication operations on the binary numbers shown below.

10111	11100	11011
+1111	-1011	x 110

2. Convert the binary number 100111000.11 to

a. octal

b. hexadecimal

Convert the decimal number, 60.5, to

a. binary

b. BCD

3. Fill in the parity bit below so that the parity of the code is ODD.

0110110_

4. Find a 5-bit representation for -5 using 2's complement representation

5. Simplify the following expression using Boolean Algebra.

$$F(wxyz) = xyz + x + \overline{(\overline{w} + \overline{x})} + \overline{(\overline{w} + \overline{x})}$$

6. For the function described by the truth table below,

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

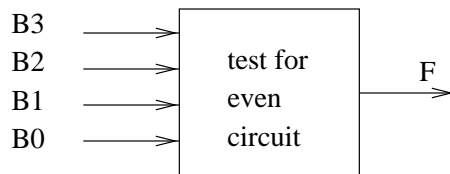
a. Write F in shorthand sum of minterm form.

b. Write F in shorthand product of maxterm form.

c. Use a K-map to minimize F to a SOP form.

d. Draw a NAND-NAND circuit to implement the minimum SOP form. You may assume that all variables and their complements are available.

7. The circuit below accepts BCD inputs for decimal digits 0 through 9. The output, F, is 1 only if the BCD input is even. Find a minimum SOP expression for F.



8. The function below is one (of several) minimum SOP expressions for the function shown in the K-map. Circle the regions that correspond to the expression shown.

		CD			
		00	01	11	10
AB	00	1	1	0	1
	01	0	1	1	0
	11	0	0	1	0
	10	1	0	1	0

$$F = \bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{C}D + BCD + ACD$$

9. Fill in the truth table for a combinational circuit with 4 inputs (R1,G1,R2,G2) and 3 outputs (F1,F2,F3). The inputs, R1,G1,R2,G2, represent the status of the red and green lights for a traffic light at the intersection of two roads, route 1 and route 2. If an input is 1, then that light is on, when it is 0, it is off. You may assume that when both red and green are off for a particular road, then the yellow light for that road is on. You may also assume that red and green lights for a particular route will never be on at the same time.

F1 is the "hazard" function, and will be high whenever the lights are in a hazardous condition (any condition that allows traffic to flow on both roads).

F2 is the "deadlock" function and will be high whenever the lights are such that traffic stops both ways.

F3 is a "normal" function and will be high when traffic is flowing in either direction.

R1	G1	R2	G2	F1	F2	F2
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

10.

a. Use DeMorgan's theorem to find the complement of G.

$$G = X(Y' + Z) + X'Y$$

b. Find the truth table for G.

11. For the function described by the truth table below,

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Write F in minimum product of sum form.

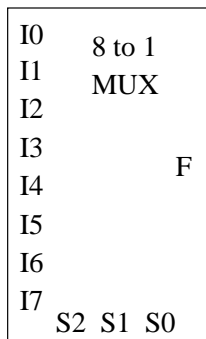
12. Show a minimized 2-level NAND implementation of the following function. You may assume that all variables and their complements are available.

$$F = A(B + C)$$

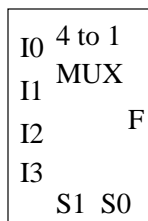
13. Given the following function

$$F(A, B, C) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6$$

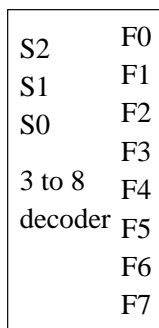
a. Implement with the 8 to 1 MUX shown below.



b. Implement with the 4 to 1 MUX shown below.



c. Implement with the 3 to 8 decoder shown below.



14. a. Complete the function table for the priority encoder shown below. The input with the highest subscript has the highest priority.

I3	I2	I1	I0	F1	F0	V
0	0	0	0	0	0	0
0	0	0	1	0	0	1

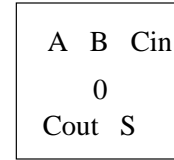
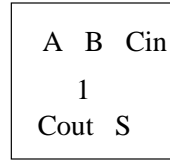
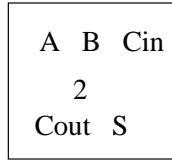
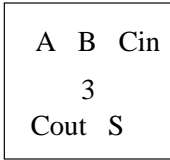
4 to 2
priority
encoder

I0	F1
I1	F0
I2	
I3	V

b. Given that the following inputs are applied to the encoder, give the outputs.

I_3	I_2	I_1	I_0	F_1	F_0	V
1	0	1	0			
0	0	1	1			
0	1	1	0			

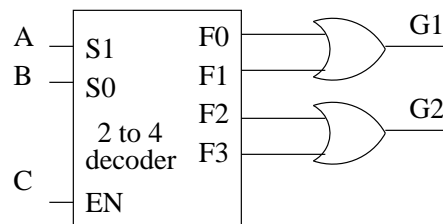
15. a. Show how the 4 full adders shown below can be connected to implement a 4-bit adder that adds $A_3A_2A_1A_0$ to $B_3B_2B_1B_0$ and produces $S_3S_2S_1S_0$ and a carry-out C_4 .



b. Provide the truth table for a full adder.

c. In part a, which full adder (3, 2, 1, or 0) could be replaced with a half adder? _____
Why?

16. Fill in the truth table for the circuit below.



A	B	C	G_1	G_2
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		