EER-018 Introduction to Digital Computers
Laboratory 5
TTL Latches, Flip-flops and Registers

Objectives:

1. To introduce the concept of sequential circuits by examining latches and flip-flop circuits.
2. To understand the common application of SR latches to the switch bounce problem.
3. To learn about the behavior and application of the 74175 Quad D flip-flop.

Equipment:

- 1 Lab Setup:
  - Protoboard with power supply
  - switches,wires,LEDs,resistors
- TTL chips:
  - 7400 - Quad NAND gate
  - 74175 - Quad D Flip-Flops

Reference:

- Datasheet for 7400 and 74175 components (YOU MUST GET THIS DATASHEET FROM THE LAB WEB LINK)

Prelab:

1. Draw pin diagrams for Procedure, part 1, part 6, part 7.
2. Complete the timing diagram on the reference page.

Procedure:

1. Connect two NAND gates as shown in class to construct an SR latch. Connect toggle switches to the S and R inputs and LEDs to outputs Q and Q'.
2. Verify that the "set" and "reset" inputs produce the expected results.
3. Now set both inputs low. What are the outputs? Now try to switch both inputs simultaneously to high. What is the final state? Repeat this step several times. Do the outputs settle in the same state every time?
4. Develop a characteristic table for the SR latch based on your results.
5. Wire the **pushbutton** switch to the latch as indicated in the " debouncing circuit" on the attached reference page. Verify that you have an active low (normally high until you push the button) pulse on Q and an active high pulse on Q'.
6. Connect the active high pulse output, Q', from the switch debouncing circuit to the clock input of a 74175 D flip-flop. Connect a toggle switch to the D input and a LED to the flip-flop Q output. Verify that the flip-flop behaves as the characteristic table in the datasheet indicates. When does the output of the flip-flop change state - on the rising or falling edge of the clock? Record your results in the form of a timing diagram and a characteristic table.
7. Now make the following connections to use the 4 D flip-flops in the 74175 to create a 4-bit shift register.
   - Connect the active high pulse output, Q', from the switch debouncing circuit to the clock inputs of the 74175.
   - Connect the D1 input to a toggle switch.
   - Connect the Q_i outputs to D_{i+1} inputs (for i=1,2,3).
   - Connect the CLEAR (reset) input to a toggle switch.

- Connect LEDs to the Q1, Q2, Q3, Q4 outputs.

8. Set the CLEAR input to 0 and observe the LED outputs. Now set the CLEAR input to a 1.
9. Set the D1 input to 1 and press the pushbutton switch 5 times to produce 5 clock pulses. Record the resulting values on Q1, Q2, Q3, Q4 outputs after each clock pulse in Table 1.

clock pulses	Q1	Q2	Q3	Q4
1				
2				
3				
4				
5				

Table 1. Results of Shift Operation

10. Connect the Q4 output (pin 14) to the D1 input, and disconnect the toggle switch that was previously connected to D1.
11. Set the CLEAR input to 0 to reset the flip-flops, then press the pushbutton 9 times, recording the values on Q1, Q2, Q3, Q4 in Table 2 after each press.

clock pulses	Q1	Q2	Q3	Q4
1				
2				
3				
4				
5				
6				
7				
8				
9				

Table 2. Results of Inverted Circular Shift Operation

Question:

1. The circuit designed in step 10 is called a Johnson counter. Suppose we initialized the circuit so that the initial inputs are as follows. Fill in the sequence that would result from pulsing the clock 8 times.

clock pulses	Q1	Q2	Q3	Q4
0	0	1	1	0
1				
2				
3				
4				
5				
6				
7				
8				
9				

2. Explain how the "debounce" circuit debounced the switch to produce a reliable clock signal.

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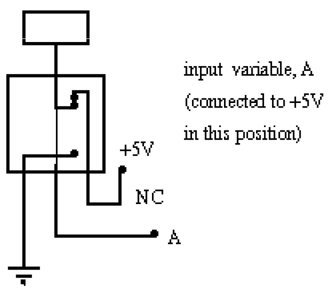
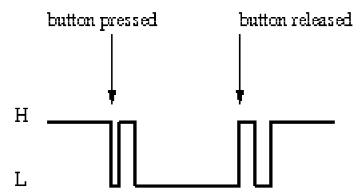
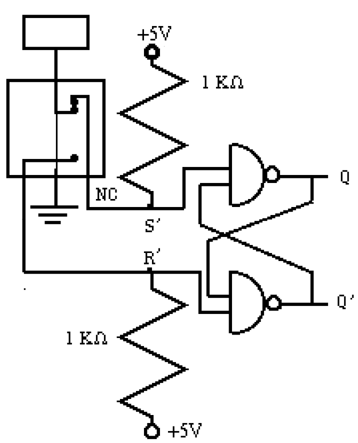
Shown below is a pushbutton switch. It is spring loaded so that if you are not pushing it, the middle pin is connected to the side pin marked NC (Normally Connected). When the button is pushed, the middle sliding contact is pressed against the other side pin contact. If we connect one of the side pins to +5V and the other to GND and use the middle pin as a variable as we do in the toggle switches, we get the following output on the middle pin when the button is pushed:

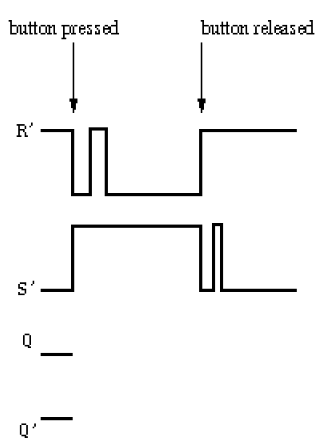




This timing diagram is blown up so the time scale is in milliseconds. As you can see, the switch does not produce a clean transition from one logic level to the other. Instead, it "bounces". Switch bounce has not been a problem in the combinational circuits that we have examined so far because the human eye cannot detect this bounce and it settles out in a matter of milliseconds. When switches are used as clock inputs to flip-flops, however, it becomes a problem because when we intend to input a single pulse, we are instead inputting several pulses. In the case of a toggle flip-flop, for example, this can result in an indeterminate final state. This is a characteristic of ALL mechanical switches and cannot be eliminated in the design of the switch itself. We CAN, however, obtain a clean, "debounced" signal from the switch by adding a " debouncing circuit".

This circuit consists simply of an S'R' latch. Examine the debouncing circuit shown below connected to the switch. Since the S'R' latch has 2 inputs, the side pins of the switch are now inputs rather than being connected directly to +5V or GND. The middle pin is connected to GND so that when the button is UP, the rightmost pin is connected to GND and the leftmost pin is connected to +5V. When the button is pressed down, the leftmost pin is connected to GND and the rightmost pin is connected to +5V. The resistors must be inserted so that +5V is never connected directly to GND. This direct connection tends to ruin power supplies.





The timing diagram for the bouncing switch outputs is given, where the initial values of Q and Q' are 0 and 1, respectively. Keeping in mind the characteristic table of the SR latch, fill in the outputs, Q and Q'. Make sure you understand why the outputs are not bouncy like the inputs.