

# EER-018 Introduction to Digital Computers

## Laboratory 6

### FSM Design

#### Objectives:

1. To practice the design and implementation of sequential circuits starting from a state diagram description.
2. To gain experience with the waveform and table output of the MAX+plus II simulator.

#### Equipment:

- Laboratory PC
- MAX+plus II

#### Prelab:

The state diagram below illustrates a 2-bit "Gray" counter. Note that as we go from state to state, only one of the outputs changes. The input UD determines the direction of the count sequence. Since the outputs are defined within the states, this is a Moore type sequential circuit.

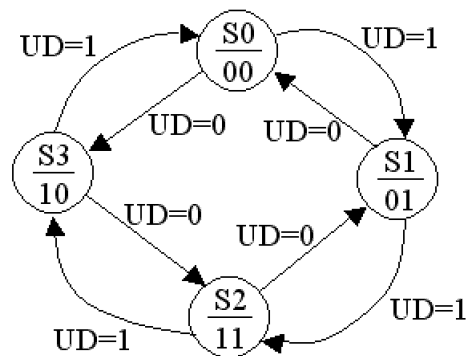


Figure 1. State Diagram for Gray Counter

1. Using the following state assignment, derive the state table from the state diagram in Figure 1.

| State | y1 | y0 |
|-------|----|----|
| S0    | 0  | 0  |
| S1    | 0  | 1  |
| S2    | 1  | 1  |
| S3    | 1  | 0  |

2. Find the next state equations for  $y1^n$  and  $y0^n$ .
3. Assuming D flip-flops for the implementation, find the equations for D1 and D0.
4. Note that the outputs of this counter are the same as the state variables  $y1$  and  $y0$ .
5. Using D flip-flops, and logic gates, draw a logic diagram for the circuit.

# Procedure:

## Circuit Entry

1. Enter the logic diagram from prelab into the MAX+plus II graphical editor.
  - o All elements can be found in the ../prim library.
  - o The Vcc element can be used for a logical 1, and the GND symbol can be used for a logical 0 if needed.
  - o Be sure to include a clock input and a reset input. Connect the reset input so that it can be used to set the initial state of the circuit to y1y0=00.
  - o Be sure to name all inputs and outputs.
  - o Label signals D1, D0, Y1 and Y0.
  - o Save the circuit often.

## Simulation

### Predicting what will happen:

1. Is your reset input active low, or active high, as you have your circuit drawn? \_\_\_\_\_
2. Give the sequence of reset and UD input values that will produce the following sequence of states.
3. Does this sequence of states test all possible state transitions in the circuit? If not, add more clock cycles to the table and fill in the inputs required to make those transitions.

| clock cycle | 0      | 1      | 2      | 3      | 4      | 5      | 6      | 7      | 8      | 9  |
|-------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|----|
| Y1 Y0       | 00---> | 01---> | 11---> | 10---> | 00---> | 10---> | 11---> | 01---> | 00---> | 01 |
| reset       |        |        |        |        |        |        |        |        |        |    |
| UD          |        |        |        |        |        |        |        |        |        |    |

Table 1 - Simulation Test Sequence

### Performing the simulation:

To verify that our circuit works as designed, we will now compile and simulate the circuit.

1. Remember to set the project to the current file before compiling.
2. Open the waveform editor and add the circuit inputs and outputs.
3. Select the clock signal and then click on the clock tool (4th button from bottom on the left side). Set the clock period to 100ns.
4. Zoom out so that all 10 clock cycles are visible on the waveform.
5. Using the mouse to select regions and the 0 and 1 signal force buttons on the left, set the reset and UD inputs so that the circuit will transition through the sequence of states in Table 1.
6. Run the simulator and record the inputs and outputs below for each clock cycle.

| Clock cycle | Reset | UD | Y1 | Y0 |
|-------------|-------|----|----|----|
| 0           |       |    |    |    |
| 1           |       |    |    |    |
| 2           |       |    |    |    |
| 3           |       |    |    |    |
| 4           |       |    |    |    |
| 5           |       |    |    |    |
| 6           |       |    |    |    |
| 7           |       |    |    |    |
| 8           |       |    |    |    |

Table 2. Simulation Results

Compare your results with the state diagram specification. Once you are satisfied that your circuit works correctly, save the waveform and print a copy of the waveform and the circuit.

### Tabular Output

MAX+plus II provides a tabular view of the output as a function of time as well. This is often useful to obtain detailed timing analysis.

1. Choose "Create Table File" from the File menu. Use the same file name as your circuit and waveform files, but with a .tbl extension.
2. Open the file and notice that there are three major parts of the file. The first part is comments about the intellectual property rights of Altera. Ignore this. The second part specifies the inputs and outputs of the file, the unit of time used, and the radix. The last part is called the "pattern" part of the file, and it gives the time of each signal transition during the simulation.
3. Notice that the waveform file and the table file contain the same information, in different formats.

### Exercise

Design a sequence detector circuit with input X, and output Z, that detects the sequence 001. Below is a sample input and output sequence for the detector:

|          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|----------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| input X  | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| output Z | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

1. Draw a Mealy state diagram that represents the behavior of the circuit. The output, Z, should be defined on the transitions between state.
2. Derive a state table from the Mealy state diagram.
3. Using D flip-flops, derive the flip-flop input equations and the output equations from the state table.
4. Using Max+Plus II, enter this circuit in the graphical editor by following the Circuit Entry procedure that you used in this lab.
5. Simulate the circuit for the input sequence shown above to verify that it works properly. Be sure to draw your inputs so they are synchronized with the clock - they should only change on the rising edge of the clock. Print the trace waveform.
6. Now change the inputs so that they are synchronized with the FALLING edge of the clock. Print this waveform and examine the timing of the transitions on the Z output. When do they occur, relative to the clock transition? How does this differ from the timing of the output transitions on the Gray counter circuit?
7. Explain why the two circuits have different timing.

Be sure to include the following items when you submit the results of this exercise.

- A title page that follows the format used for lab reports.
- A clear presentation of all steps of your circuit design work.
- A printout of your circuit.
- A printout of the waveform that shows the correct results for all possible inputs.
- Answers to all questions posed in the exercise.

Attach the prelab results, lab handout, and circuit and simulation printouts to your lab exercise.

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