

EE-18 Exam 2
Fall, 2003
Prof. Traver

Name: _____

1. Write a VHDL concurrent statement to implement the Boolean function:

$$P = (AB' + C)(B \oplus D)$$

2. Draw the logic circuit that is described by the following structural VHDL description.

```
entity circuit is
port ( X, Y, Z : in bit; F, G: out bit);
end circuit;

architecture exam_problem of circuit is

component AND is
port (A,B: in bit; C out bit);
end component;

component OR is
port (A,B: in bit; C out bit);
end component;

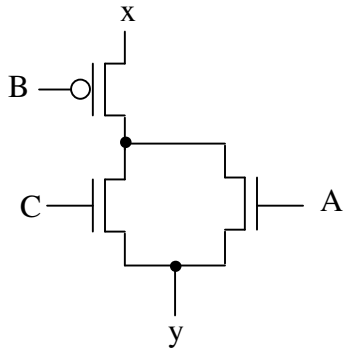
signal S1, S2 : bit;

begin

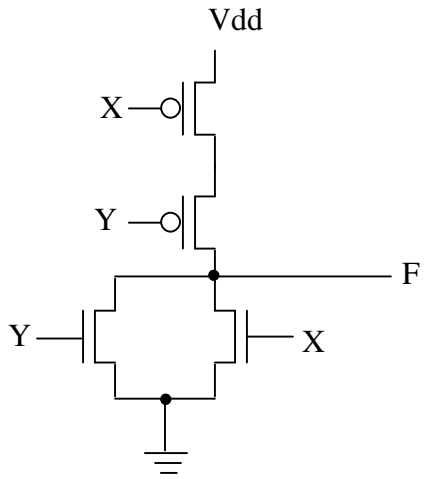
G1: AND port map (X, Y, S1);
G2: AND port map (Y, Z, S2);
G3: OR port map (S1, S2, F);
G4: AND port map (S1, Z, G);

end exam_problem;
```

3. Give all values of the input variables that will connect nodes x and y together.

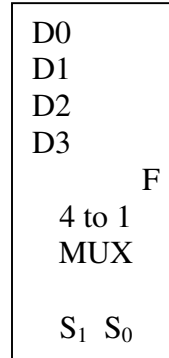


4. Give the truth table for the CMOS circuit below with inputs X, Y and output F.

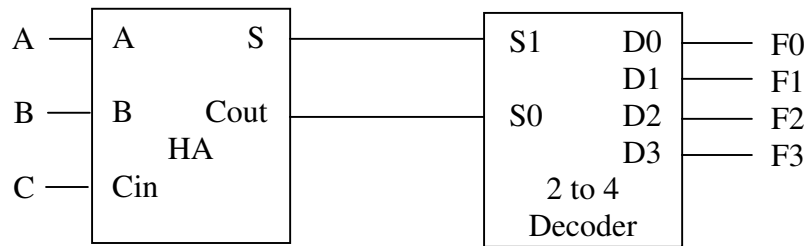


5. Use the multiplexor shown to implement the function F.

$$F(a,b,c) = \sum m(0,4,5,7)$$



6. In the circuit below, a Half-Adder (HA) circuit is connected to a 2 to 4 decoder. Fill in the resulting function table for the overall circuit.

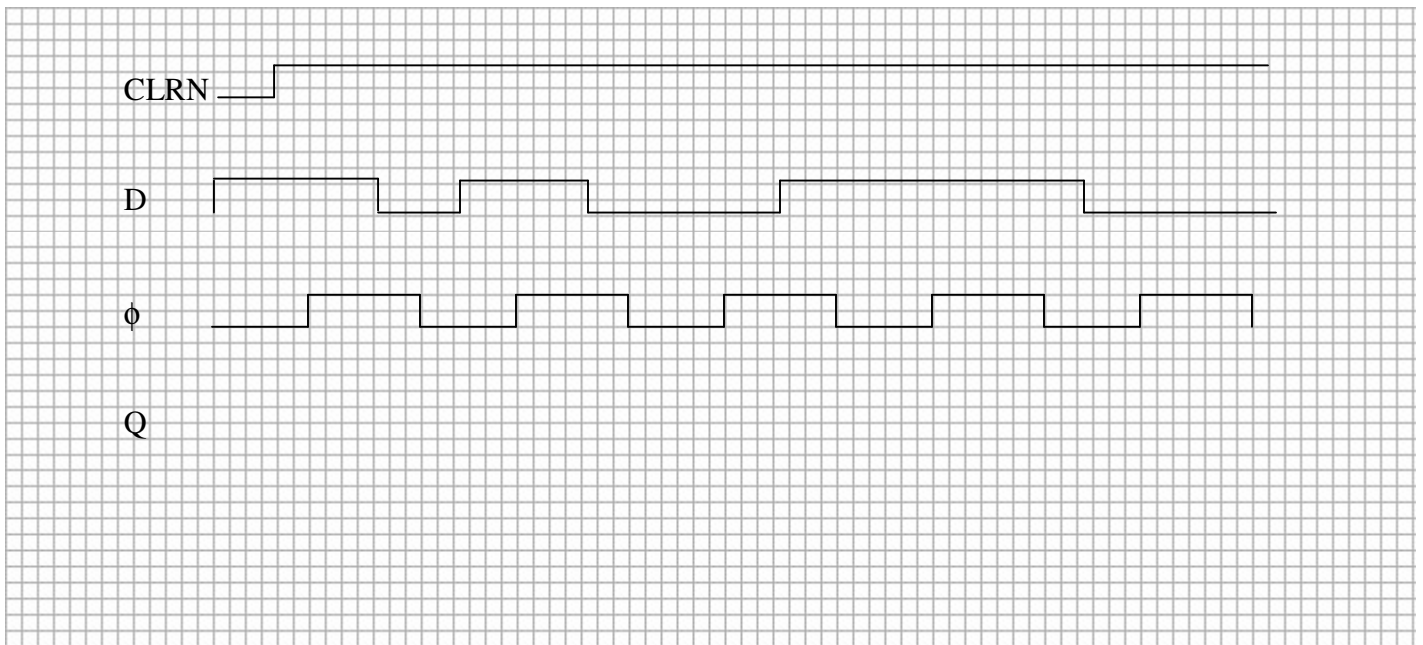
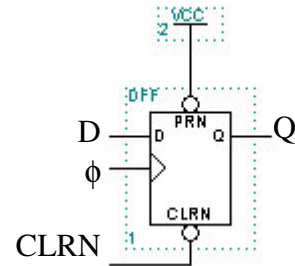


A	B	C	F0	F1	F2	F3

7. Perform the following subtraction by translating to binary (8-bits), and applying the 2's complement approach.

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8. Fill in the waveform for the output of the flip-flop shown.



9. An 8-bit register is initially loaded with the value 01101101. Give the contents of the register (in binary) after the following operations are performed:

a) ROL 3

b) SHL 2

c) ROR 1

10. Given a RAM module of size 512 x 8.

a) How many address lines does it have?

b) How many data lines does it have?

c) How many of these 512 x 8 RAMs are needed to build a 1K x 16 RAM?