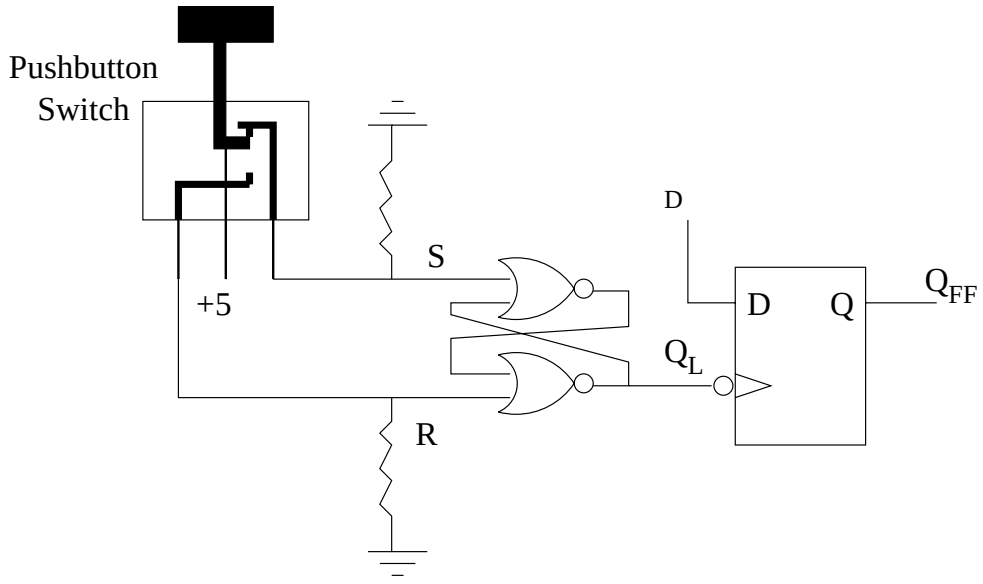
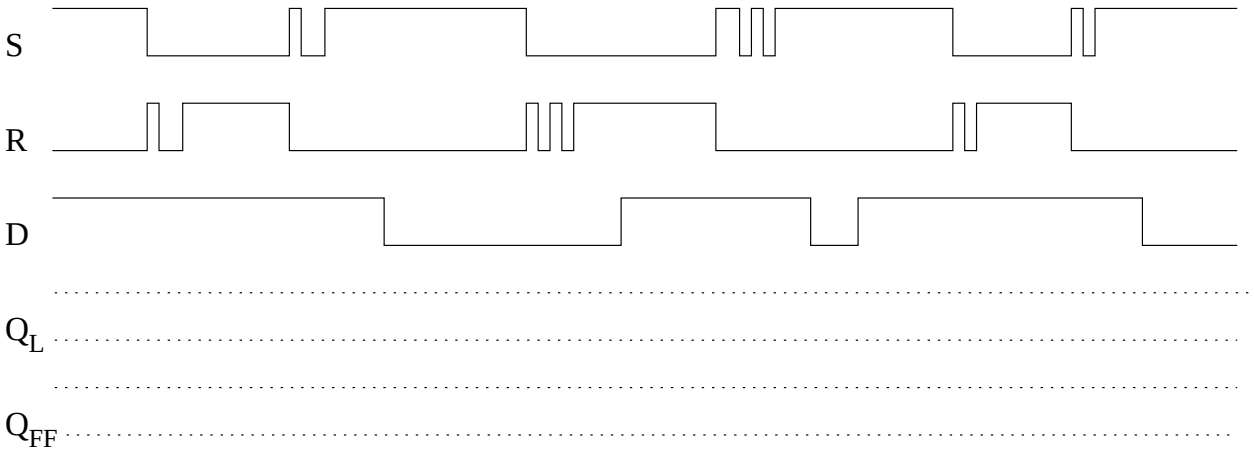
EE-18 - Exam 2
Fall 1997 - Prof. Traver

Name _____

Complete 7 of the 8 problems. Mark the one you do NOT want graded.

1. Fill in the timing diagram for Q_L and Q_{FF} below.





2. Suppose we need to build a 64M x 4 RAM module with some number of 16M x 4 RAM chips.

a. How many 16M x 4 RAMS are needed? _____

b. How many address lines must be used to access the 64M x 4 RAM? _____

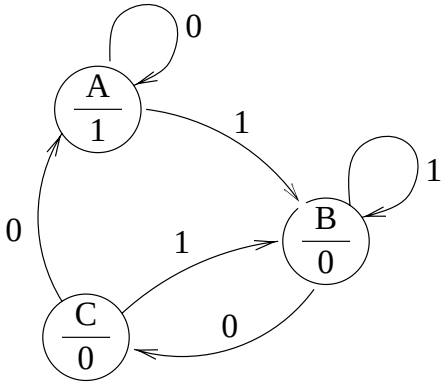
c. How many data input lines are required? _____

d. How many address lines are connected to the address inputs of all chips? _____

e. How many lines must be decoded for the chip select inputs?_____ Specify the size of the decoder._____

3. A circuit has one input, X, and one output, Z. It can be described by the state diagram shown below.

a. Is this a Mealy or Moore circuit description?_____



b. Find the state table.

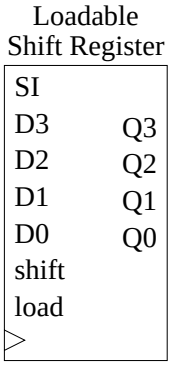
4. Using D flip-flops, find the circuit that implements the transition table shown below.

current state	next state A^nB^n		output
AB	X=0	X=1	Z
00	01	10	1
01	00	11	0
10	11	00	0

5. Suppose we want to design a switch-tail counter that counts in the following repeating sequence:

Q_3	Q_2	Q_1	Q_0
1	0	1	0
1	1	0	1
0	1	1	0
1	0	1	1
0	1	0	1
0	0	1	0
1	0	0	1
0	1	0	0

Show the connections required to accomplish this with the loadable shift register shown below. The function table for this shift register is provided. You may use additional gates if necessary.



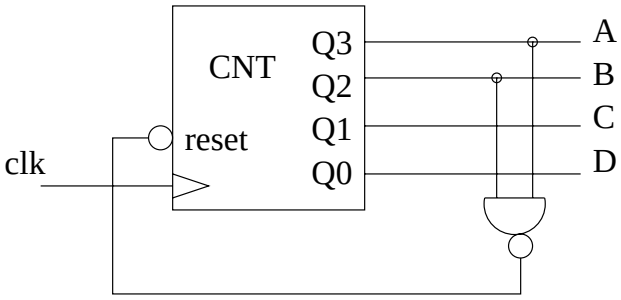
Function Table

load	shift	$Q3^n$	$Q2^n$	$Q1^n$	$Q0^n$	function
0	0	Q3	Q2	Q1	Q0	hold
0	1	SI	Q3	Q2	Q1	shift right (down)
1	X	D3	D2	D1	D0	parallel load

6. Give the count sequence for the following counter that is configured from a binary counter, CNT. Note that the reset input is ASYNCHRONOUS.

Count Sequence

A B C D



7. Give the size of the ROM required to implement the following functions:

a. A 10-input priority encoder. Remember the encoder will have a "valid" output as well as the encoded outputs.

b. A code converter that converts a 2-digit BCD number to its ASCII code. Each ASCII character is encoed in 7-bits.

c. A combinational binary multiplier that multiplies two 5-bit numbers.

8. The following two functions will be implemented with a PLA. Give the PLA programming table for the implementation. Be sure to minimize the size of the PLA by minimizing the number of AND terms required. Consider using both uncomplemented and complemented outputs.

$F(ABC) = m_0 + m_1 + m_2 + m_4 + m_6$
$G(ABC) = m_4 + m_5 + m_6 + m_7$