

**EE -18**  
**Introduction to Digital Computers**  
**Exam 2**  
**Fall, 1998**  
**Prof. Traver**

1. (14 points)

a. Fill in the function tables for the following latches and flip-flops.

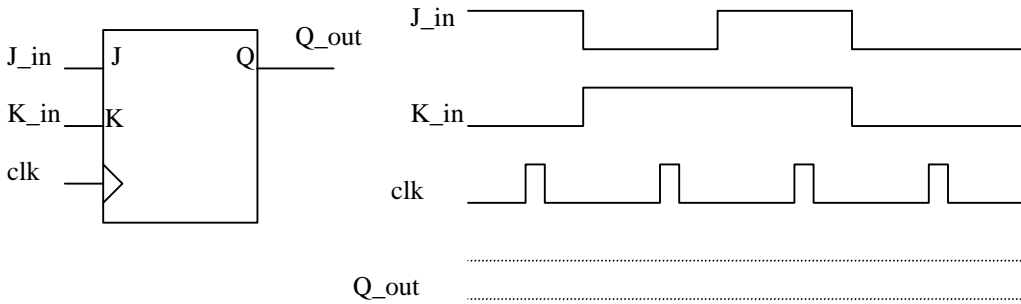
D flip-flop	
D	$Q^n$
0	
1	

JK flip-flop		
J	K	$Q^n$
0	0	
0	1	
1	0	
1	1	

SR-latch		
S	R	$Q^n$
0	0	
0	1	
1	0	
1	1	

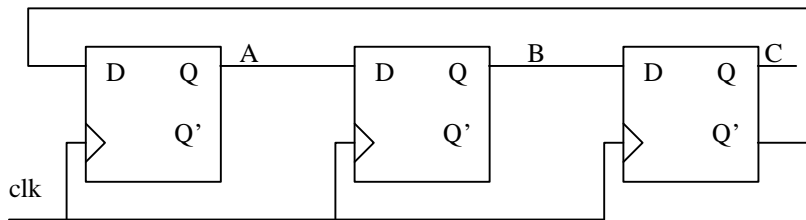
T flip-flop	
T	$Q^n$
0	
1	

b. Fill in the timing diagram for the JK flip-flop output.



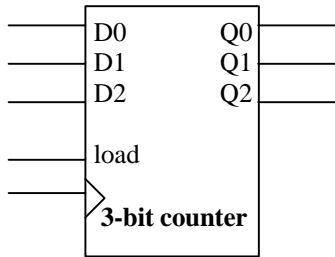
2. (14 points) Give the sequence generated by the following circuit after all the flip-flops are reset to zero.

A B C



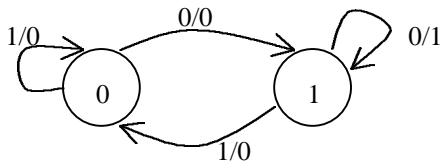
3. (14 points) Modify the following 3-bit counter so that it is a mod 7 counter that counts in the repeating sequence 000, 001, 010, 011, 100, 101, 110, 000 ... The function table of the counter is given. Additional logic will be needed. Be sure to define all inputs.

load	clk	function
0	↑	count up
1	↑	load inputs



4. (14 points)

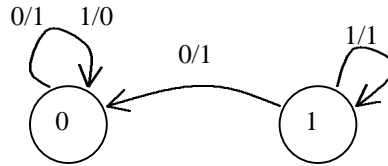
a. Given the state diagram below, draw the corresponding state table. The input is X and the output is Z.



b. Is this a Mealy or Moore state diagram? \_\_\_\_\_

5. (14 points) A state diagram and the corresponding state table are given below. Find the circuit that implements these. Use a D flip-flop. Be sure to label all inputs, outputs and state values.

current state	input	next state	output
Q	x	Q <sup>n</sup>	Z
0	0	0	1
0	1	0	0
1	0	0	1
1	1	1	1



6. (14 points) Given the partial PLA table below, write equations for F and G.

A	B	C	(T) (C)	
			F	G
0	1	-	1	0
1	-	1	1	1
1	0	0	0	1
0	-	-	0	1
1	1	-	1	0

7. (14 points)

a. Give the size of a ROM with 8 address lines and 4 data lines. \_\_\_\_\_

b. What size ROM is required to implement a 4-bit adder? \_\_\_\_\_

c. Give the number of address lines and data lines for a 1K x 4 ROM. \_\_\_\_\_

d. Is a ROM a combinational or sequential module? \_\_\_\_\_ (hint: it can be used to implement a 4-bit adder)

8. (5 points extra credit) Show how 256 x 4 RAMs would be connected to form a 1M x 8 memory module. Be sure to label all inputs and outputs of the module, and all inputs and outputs of the individual RAMs.