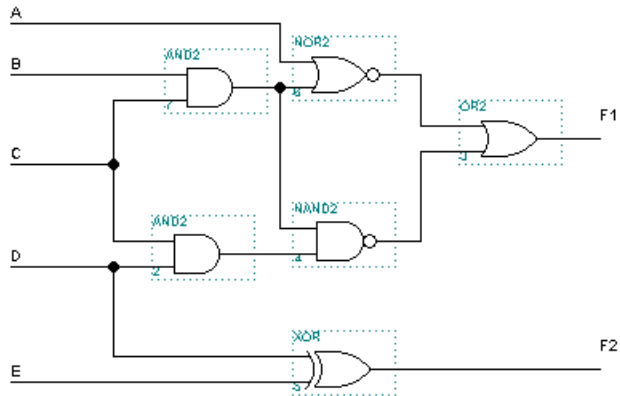


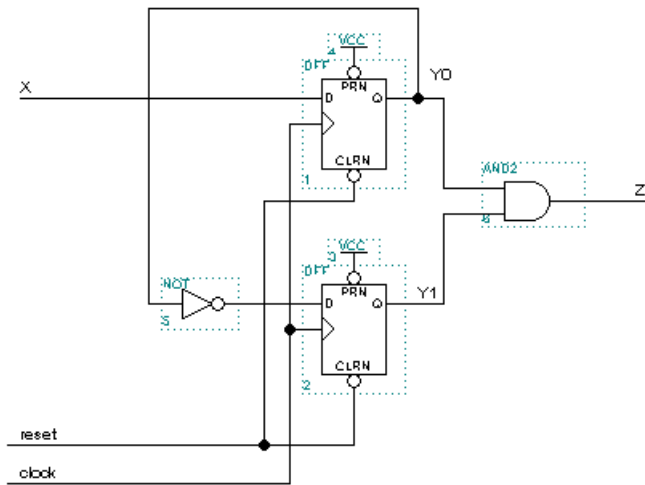
EE-18 Introduction to Digital Computers
Final Exam
Fall, 1998
Prof. Traver

1. Find expressions for the F1 and F2 functions in the circuit shown below. Use Boolean algebra to reduce the expressions to **sum of product** form. The expressions do **not** have to be minimized.



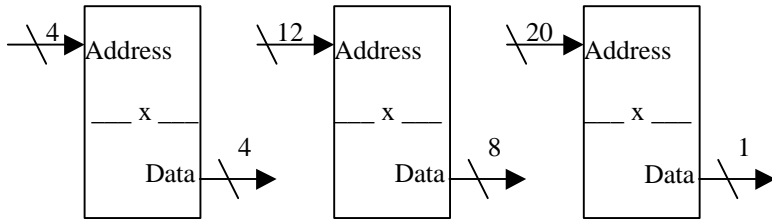
2. Design a circuit with a 3-bit number as input, and an output that is the quotient (throw away the remainder) of the number divided by 3. For example, if the input is 101 (5), then $5/3 = 1 R2$, so the output should be 01. The inputs of the circuit are B2, B1, B0 and the outputs are Q1, Q0. Your implementation should be a minimized, 2-level combinational circuit.

3. Find the state diagram for the circuit shown below.



4.

a. Fill in the sizes of the ROM modules shown below.



b. How many 256K x 8 ROM modules are required to build a 1M x 16 ROM? _____

c. Give the number of address and data lines of the following ROMs.

256 x 8 ____ address lines ____ data lines

8K x 1 ____ address lines ____ data lines

5. Implement the following function with the following modules or gates. You may assume that all variables and their complements are available.

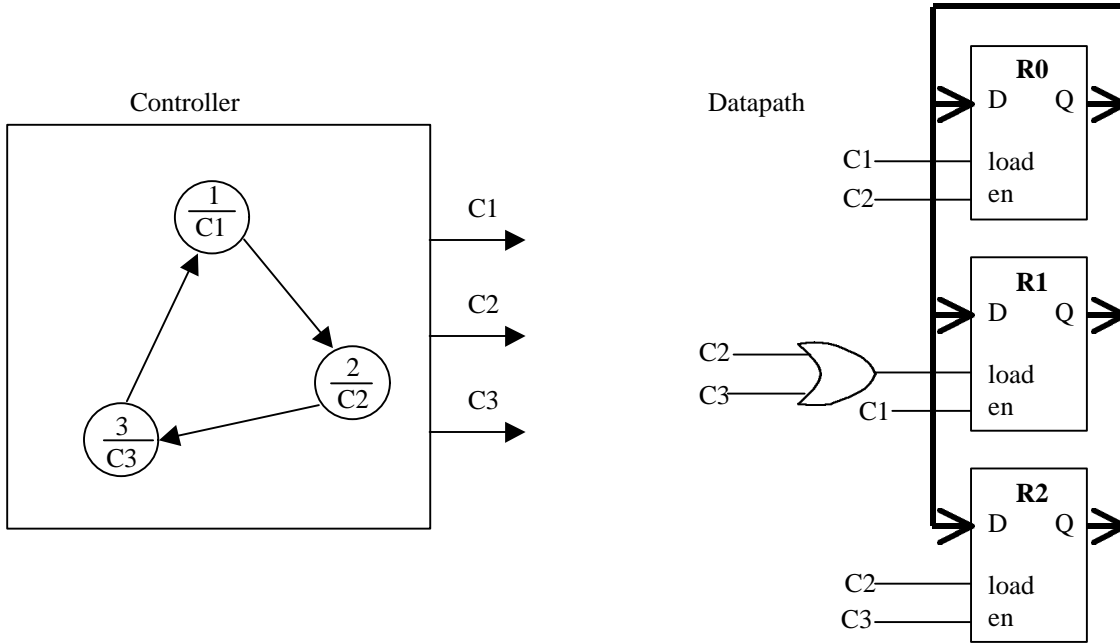
$$F(A, B, C) = \sum m_0 + m_3 + m_4 + m_5 + m_7$$

a. a 4 to 1 multiplexor

b. a 3 to 8 decoder and an OR gate.

c. all NAND gates.

6. The single-bus datapath shown below is controlled by a controller as shown. The controller has outputs C1, C2, and C3 and operates as shown in the state diagram. Give the sequence of register transfers that occur in this system.



7. Design one bit of an ALU that has the following function table.

S1	S0	cin=0	cin=1
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = A + B'$	$F = A + B' + 1$
1	0	$F = A \wedge B$	
1	1	$F = A \vee B$	

8. Show a bus-based datapath that will implement the following register transfers.

ca: $R0 \leftarrow R2, R1 \leftarrow R3$

cb: $R2 \leftarrow R1, R3 \leftarrow R2$

cc: $R2 \leftarrow R3$

9. Hand assemble the following 6805 program and give the address and machine code for each instruction in the memory table shown.

```

        ORG $300
start:  CLRX
        LDA #$C1
loop:   STA $E0,X
        INCA
        INCX
        BRA loop
    
```

Memory Address	Memory Contents

10. Analyze the following 6805 program and give the final values of A, X, and any memory locations that are modified.

```

        ORG $300
start:  LDA #$96
        STA $D0
start:  CLR $D1
        LDX #$8
        LDA $D0
next:   LSLA
        BCC skip
        INC $D1
skip:   DECX
        BNE next
done:   STOP
        ORG $7FE
        FCB start
    
```