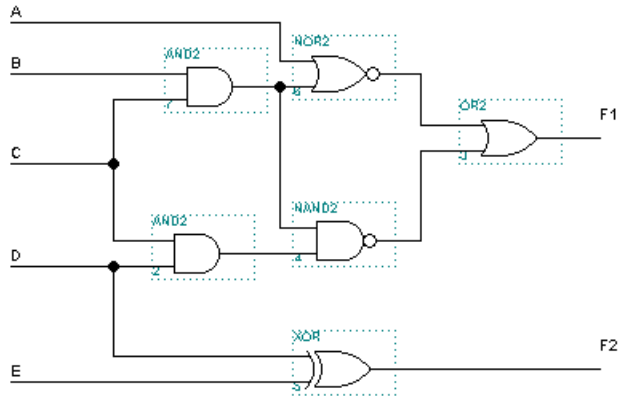


**EE-18 Introduction to Digital Computers**  
**Final Exam**  
**Fall, 1998**  
**Prof. Traver**

1. Find expressions for the F1 and F2 functions in the circuit shown below. Use Boolean algebra to reduce the expressions to **sum of product** form. The expressions do **not** have to be minimized.



$$\begin{aligned}
 F1 &= (A+BC)' + ((BC)(CD))' \\
 &= A'(B'+C') + B'+C'+D' \\
 &= A'B' + A'C' + B' + C' + D'
 \end{aligned}$$

$$F2 = DE' + D'E$$

2. Design a circuit with a 3-bit number as input, and an output that is the quotient (throw away the remainder) of the number divided by 3. For example, if the input is 101 (5), then  $5/3 = 1$  R2, so the output should be 01. The inputs of the circuit are B2, B1, B0 and the outputs are Q1, Q0. Your implementation should be a minimized, 2-level combinational circuit.

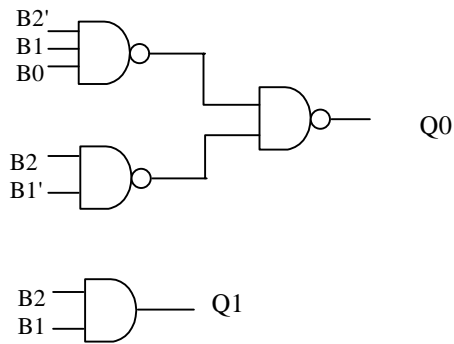
B2	B1	B0	Q1	Q0
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	1	0
1	1	1	1	0

B2 \ B1 B0	00	01	10	11
0	00	00	00	00
1	00	01	01	01

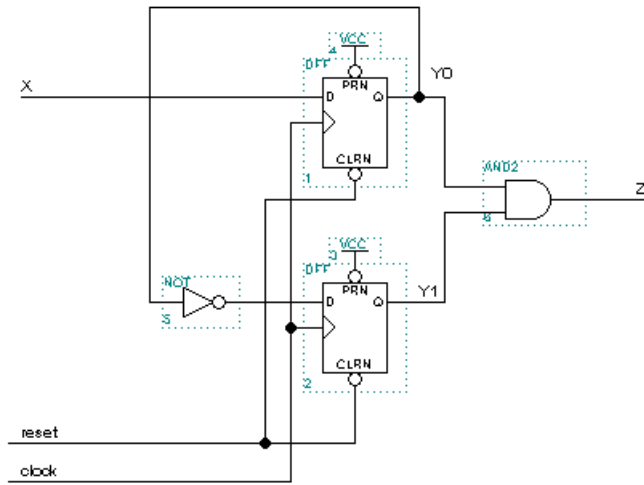
$$Q1 = B2 B1$$

B2 \ B1 B0	00	01	10	11
0	00	01	00	00
1	11	00	00	00

$$Q0 = B2 B1' + B2' B1 B0$$



3. Find the state diagram for the circuit shown below.



Flip-flop input equations:

$$D_0 = X$$

$$D_1 = Y_0'$$

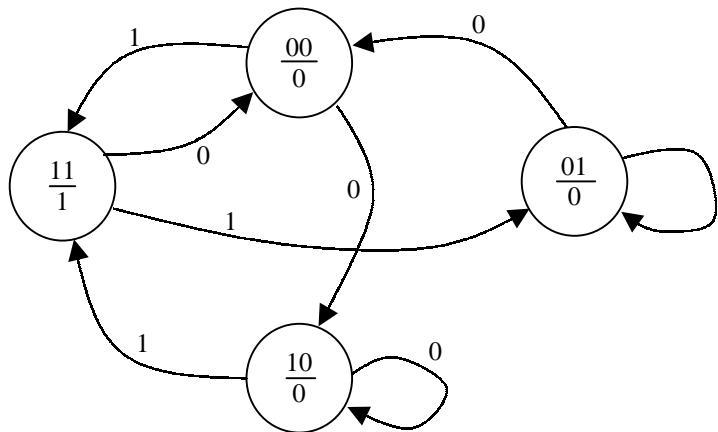
Output equation:

$$Z = Y_1 Y_0$$

State Table: Using  $Y_1^n = D_1 = Y_0'$  and  $Y_0^n = D_0 = X$

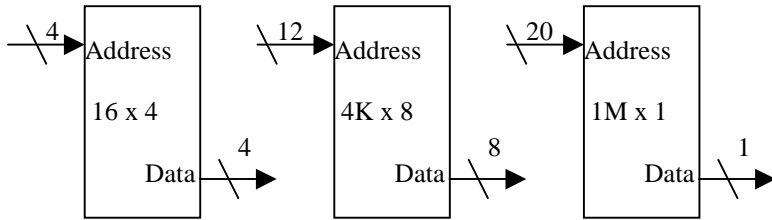
$Y_1$	$Y_0$	$x=0$	$x=1$	$Z$
0	0	10	11	0
0	1	00	01	0
1	0	10	11	0
1	1	00	01	1

State Diagram:



4.

a. Fill in the sizes of the ROM modules shown below.



b. How many 256K x 8 ROM modules are required to build a 1M x 16 ROM? 8

c. Give the number of address and data lines of the following ROMs.

256 x 8 8 address lines 8 data lines

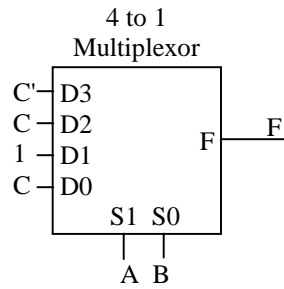
8K x 1 13 address lines 1 data lines

5. Implement the following function with the following modules or gates. You may assume that all variables and their complements are available.

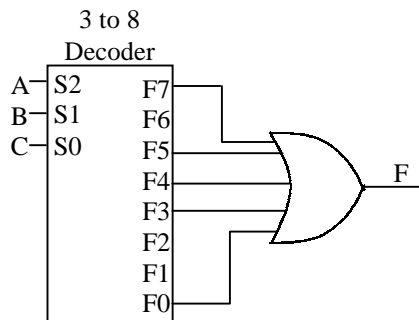
$$F(A, B, C) = \sum m_0 + m_3 + m_4 + m_5 + m_7$$

a. a 4 to 1 multiplexor

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



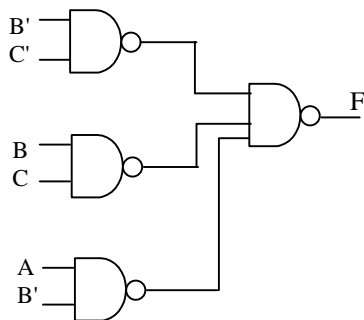
b. a 3 to 8 decoder and an OR gate.



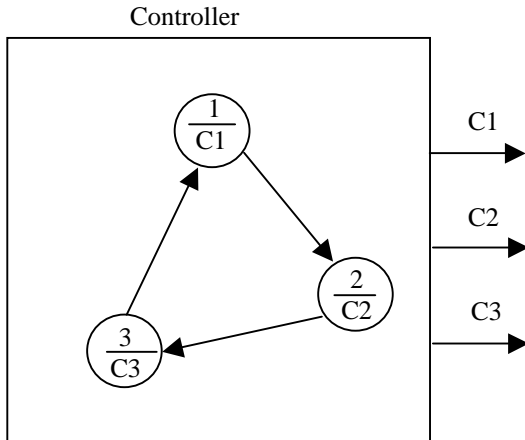
c. all NAND gates.

A	B	C	F
1	0	1	0
1	1	1	0

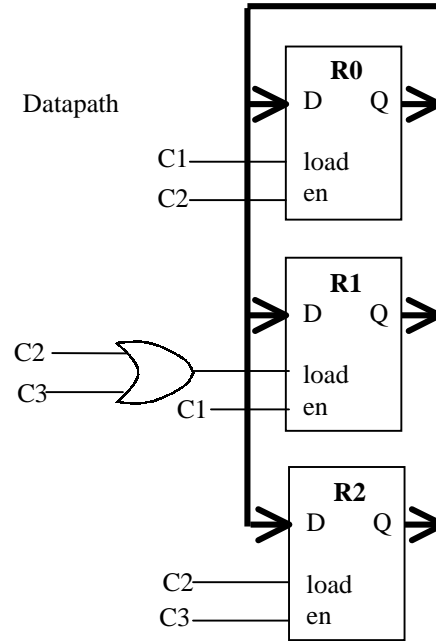
$$F = B'C' + BC + AB'$$



6. The single-bus datapath shown below is controlled by a controller as shown. The controller has outputs C1, C2, and C3 and operates as shown in the state diagram. Give the sequence of register transfers that occur in this system.



↓ C1:  $R0 \leftarrow R1$   
 C2:  $R2 \leftarrow R0, R1 \leftarrow R0$   
 ▼ C3:  $R1 \leftarrow R2$



7. Design one bit of an ALU that has the following function table.

S1	S0	cin=0	cin=1
0	0	$F = A + B$	$F = A + B + 1$
0	1	$F = A + B'$	$F = A + B' + 1$
1	0	$F = A \wedge B$	
1	1	$F = A \vee B$	

8. Show a bus-based datapath that will implement the following register transfers.

ca:  $R0 \leftarrow R2, R1 \leftarrow R3$

cb:  $R2 \leftarrow R1, R3 \leftarrow R2$

cc:  $R2 \leftarrow R3$

9. Hand assemble the following 6805 program and give the address and machine code for each instruction in the memory table shown.

```

        ORG $300
start:  CLRX
        LDA #$C1
loop:   STA $E0,X
        INCA
        INCX
        BRA loop
    
```

Memory Address	Memory Contents
300	5F
301	A6
302	C1
303	E7
304	E0
305	4C
306	5C
307	20
308	FA (-6)

10. Analyze the following 6805 program and give the final values of A, X, and any memory locations that are modified. (Final values are in bold)

	ORG \$300	A	X	Memory locations
start:	LDA #\$96	96 (10010110)	8	D0 = 96
	STA \$D0	2C (00101100)	7	D1 = 0,1,2,3,4
start:	CLR \$D1	58 (01011000)	6	
	LDX #\$8	B0 (10110000)	5	
	LDA \$D0	60 (01100000)	4	
next:	LSLA	C0 (11000000)	3	
	BCC skip	80 (10000000)	2	
	INC \$D1	<b>00 (00000000)</b>	<b>1</b>	
skip:	DECX		<b>0</b>	
	BNE next			
done:	STOP			
	ORG \$7FE			
	FCB start			