

HEP SOFTWARE SELECTION FORM 2002-2003

MENTOR GRAPHICS CORPORATION - HIGHER EDUCATION PROGRAM

Please use this form to select the software you plan to use for teaching or academic research. Also note this information in the software required section of the Curriculum Information Form. For more detailed information on the products listed below visit <http://www.mentor.com/products/>

Design Category 1 : \$504

IC Design & Verification

Custom IC Design

- Design Architect – IC** (UNIX, LINUX)
Provides the schematic capture capabilities of Design Architect integrated into the IC design flow, and includes Design Viewpoint Editor (DVE), Component Interface Browser (CIB), EldoNet and IC Parts Library.
- ICgraph Basic** (UNIX, LINUX)
ICgraph for polygon editing.
- IC Station SDL** (UNIX, LINUX)
Includes all of the functionality ICgraph Basic, and adds a hierarchical, schematic-driven layout environment to create IC layouts based on information from a logic source, plus ready-to-use parameterized device generators for digital and analog layout design.
- Hotplot** (UNIX, LINUX)
Provides the schematic capture capabilities of Design Architect integrated into the IC design flow, and includes Design Viewpoint Editor (DVE), Component Interface Browser (CIB), EldoNet and IC Parts Library.
- AutoCells** (UNIX, LINUX)
Standard cell placement and routing, up to 4 layers of metal.
- Back Annotation** (UNIX, LINUX)
Enables back annotation of parasitics to non-MGC systems from AutoCells and/or MicroPlan.
- Clock Tree** (UNIX, LINUX)
Reduces clock skew for logic built with AutoCells.
- Timing Driven Layout** (UNIX, LINUX)
Enhances circuit performance of logic built with AutoCells and/or MicroPlan.
- ADMS** (UNIX, LINUX)
ADVance MS is the industry's first mixed-signal simulator that brings together digital and mixed-signal standard HDL's with SPICE in a single environment (Verilog-AMS / VHDL-AMS).
- Mach TA, SimWave** (UNIX, LINUX)
Delivers fast, accurate, high capacity, transistor-level circuit simulation for timing and power analysis of DSM and mixed-signal IC designs (SimWave viewer).
- Mach TA, nWave** (UNIX, LINUX)
Delivers fast, accurate, high capacity, transistor-level circuit simulation for timing and power analysis of DSM and mixed-signal IC designs (nWave viewer).
- Artist Link** (UNIX)
Brings the industry's leading Eldo transistor-level simulator and the Eldo-ModelSim mixed-signal simulator to the Cadence Affirma Analog Artist environment.
- Xelga Waveform Processor** (UNIX, LINUX)
Graphical postprocessor providing waveform viewing of analog and mixed-signal simulation results.
- ADVance CommLib** (UNIX, LINUX)
Libraries of telecommunications-oriented behavioral templates for use with ADVance MS simulator.
- CommLib** (UNIX, LINUX)
Libraries of telecommunications-oriented behavioral templates for use with AccuSim, Eldo and Continuum simulators.
- Accuparts** (UNIX, Windows NT)
Analog Component Library which contains detailed models of more than 11,000 off the shelf Analog/Mixed Signal components.

Physical Verification and Manufacturability

- Calibre** (UNIX, LINUX)
Complete IC physical verification, manufacturability and resolution enhancement suite.
- xCalibrate** (UNIX)
Rules file generator for xCalibre.
- xCalibre RCC** (UNIX, LINUX)
Parasitic extraction tool that not only provides accuracy and performance, but also delivers data in usable formats for post-layout analysis tools.

Analog/Mixed Signal Simulation

- Eldo** (UNIX, LINUX)
Provides both classical (Newton-Raphson) and advanced (OSR and IEM) algorithms for SPICE-level analysis of the most complex circuits.

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Design Category 2 : \$504 HDL, DFT, HW/SW Co-Design

FPGA/PLD Design

- HDL Designer Pro** (UNIX, LINUX, Windows 98/2000/NT)
Complete tool suite for HDL design, analysis and management. In addition, HDL Designer Series supports all popular simulation and synthesis tools..
- Leonardo Spectrum Level 3 & Leonardo Insight** (UNIX, Windows 98/2000/NT)
A single synthesis environment for creating PLDs, FPGAs, or ASICs in VHDL or Verilog.
- ModelSim SE MixedHDL** (UNIX, LINUX, Windows 98/2000/NT/XP, IBM AIX)
Industry leading HDL Simulator for both VHDL, Verilog and Mixed-HDL Design with performance analyzer and code coverage verification utilities.
- FPGA Advantage** (UNIX, Windows 98/2000/NT)
Complete flow for FPGA design. This package contains HDL Designer Graphics, ModelSim SE MixedHDL, Leonardo Spectrum Level 3, and Leonardo Insight.

Design-for-Test

- MBISTArchitect** (UNIX)
Automates the creation of built-in self-test structures to ASICs/ICs that contain memories.
- BSDArchitect** (UNIX)
Provides automatic boundary scan synthesis, design and verification to incorporate industry standard IEEE 1149.1 or 1149.1a into ASIC/IC designs.
- DFTAdvisor** (UNIX)
Provides testability analysis, comprehensive DFT rule checking and test synthesis of full and partial-scan designs.
- FastScan** (UNIX)
Industry's premier automatic test pattern generation tool, creates high-quality tests for ASICs and ICs using full or structured partial scan.
- FlexTest** (UNIX)
Test pattern generation for optimal test coverage for non-scan, partial-scan or full-scan designs.

Hardware/Software Co-Design

- Seamless** (UNIX, LINUX)
Delivers high power, high validity co-verification for all of today's embedded processors, reducing the risk of integration errors, and improving time-to-market.
- Seamless PSP**
Seamless processor support packages (PSPs) available upon request. Please include your selection with this form. For a complete PSP list, visit http://www.mentor.com/seamless/psp/app_tabl.htm

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Design Category 3 : \$504

PCB Systems

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Expedition Flow

- DesignView** (Windows 98/2000/NT)
Design-centric environment for tracking entire PCB system design with all of its associated data (Design Capture + configuration management and tool launching).
- FPGA Boardlink** (Windows NT)
Automates placement and wiring of the FPGA symbol within the board schematic, reducing the process from days to seconds.
- IS_Analyzer** (UNIX, Windows NT)
Signal integrity and delay analysis for high-speed board design.
- PCB Planner** (Windows NT)
Facilitates initial placement and routing of critical components and interconnect.
- PCB Viewer** (Windows NT)
Read-only display environment allows a design to be concurrently viewed while it is in progress.
- TAU** (UNIX, Windows NT)
Performs exhaustive worst case timing analysis and verification on designs using an advanced symbolic timing methodology, which eliminates false paths typically reported in standard static timing tools.
- Expedition PCB & PCB Browser** (Windows 98/2000/NT)
Layout, analysis, and manufacture of highly-complex PCBs based upon AutoActive™ which simplifies the design process while ensuring high quality, manufacturable results.
- CAM Output Manager** (Windows 2000/NT)
Fully automates the manufacturing output process, drastically reducing the time to generate data when time is paramount - at the end of the design process.
- Library Manager** (Windows NT)
Provides a central location to create, edit and manage library data.
- Parts Manager** (Windows NT)
Management and retrieval of the critical electronics component information needed to build a firm foundation for the design environment.

Board Station Flow

- Board Architect** (UNIX, Windows NT)
Advanced schematic design entry tool for the PCB design process.

- Design Architect** (UNIX)
Complete set of advanced editing features provides the ideal front end for your PCB, ASIC, FPGA or IC design process.
- AccuSim II** (UNIX)
Analog simulator performs complete analysis from top-down to bottom-up of the most challenging IC, board and system designs.
- AutoTherm** (UNIX)
Board-level thermal analysis software.
- Continuum** (UNIX)
Provides mixed-signal simulation with AccuSim II, QuickSim II, and ModelSim.
- QuickSim II** (UNIX)
High capacity, high performance, gate-level simulation kernel for ASIC and board simulation.
- QuickSim Pro** (UNIX, Windows NT)
Provides simulation support of VHDL, Verilog, and SPICE models through the integration with ModelSim and AccuSim II.
- TAU** (UNIX, Windows NT)
Performs exhaustive worst case timing analysis and verification on designs using an advanced symbolic timing methodology, which eliminates false paths typically reported in standard static timing tools.
- IS_Analyzer, IS_Floorplanner, IS_MultiBoard, IS_Optimizer, IS_Synthesizer** (UNIX, Windows NT)
The Interconnect Synthesis (IS) Series, powered by ICX technology, offers a "best-in-class" high-speed system design and verification environment.
- Board Station** (UNIX, Windows NT)
Unites the power and convenience of automation with the flexibility and precision of innovative, interactive features, enabling complete control of the PCB design process.
- BPL-CAD** (UNIX, Windows NT)
Board Process Library – An Integrated, process-oriented part library.
- BPL-Dig Analysis** (UNIX, Windows NT)
Board Process Library – An Integrated, process-oriented part library with a digital analysis option.
- HDLWrite** (UNIX)
HDLWrite significantly speeds the process for generating HDL from the schematic for both hierarchical and flat designs, allowing rapid turnaround on design changes during circuit debug cycles.

System Modeling

- SystemVision** (Windows 2000/NT)
Combines the power of IEEE standard VHDL-AMS language with the industry standard SPICE format to provide a computer-aided prototyping environment.

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Design Category 4 : \$504

Special Interest

WorkXpert™ Electronic Design Process Management

- FlowXpert** (UNIX, Windows 2000/NT)
A runtime, multi-user process manager . Deploy and manage the execution of established best design practices throughout your engineering organization.
- ProjectXpert** (UNIX, Windows 2000/NT)
Track and monitor project status and progress. Project administration for WorkXpert.
- XpertBuilder** (UNIX, Windows 2000/NT)
Create visually intuitive standardized flows to capture best design practices for reuse and improvement.

Harness Systems

- Logical Cable** (UNIX)
Graphical connectivity editor with extensive capabilities to define, manage and quickly evaluate the impact of today's complex electromechanical design decisions.
- DC Analyzer** (UNIX, Windows NT)
Accelerates design verification tasks by analyzing logical cabling designs for steady state DC operating conditions.

Static Timing Analysis

- SST Velocity** (UNIX)
Full-chip static timing analyzer.